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| | Subclass |
| Class | ISSUE CLASSIFICATION |

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U.S. **UTILITY** Patent Application

O.I.P.E.	PATENT DATE
SCANNED TR2 Q.A.	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/886577		365		2818	

APPLICANTS Richard Roy

TITLE Simultaneous access and cache loading in a hierarchically organized memory circuit

ISSUING CLASSIFICATION

ORIGINAL			CROSS REFERENCE(S)							
CLASS	**SUBCLASS**		**CLASS**	**SUBCLASS (ONE SUBCLASS PER BLOCK)**						
INTERNATIONAL CLASSIFICATION										
								☐ Continued on Issue Slip Inside File Jacket		

☐ **TERMINAL DISCLAIMER**	**DRAWINGS**			**CLAIMS ALLOWED**	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner) (Date)			**NOTICE OF ALLOWANCE MAILED**	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	(Primary Examiner) (Date)			**ISSUE FEE**	
				Amount Due	Date Paid
☐ The terminal ____months of this patent have been disclaimed.	(Legal Instruments Examiner) (Date)			**ISSUE BATCH NUMBER**	

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